What Is Claimed Is:

1. A memory system having a memory controller and a plurality of memory modules connected by way of a plurality of wirings on a mother board, comprising a socket having a plurality of socket pins branched from one point,

wherein said wirings on said mother board are connected to each of said plurality of memory modules by using said socket, and

wherein said memory controller is connected to each of said plurality of memory modules in an equal distance.

2. A memory system according to Claim 1, wherein each of said plurality of memory modules is mounted in a radial form on said mother board by way of said plurality of socket pins of said socket.

3. A memory system according to Claim 1, wherein each of said plurality of memory modules is mounted in parallel to said mother board by way of said plurality of socket pins of said socket.

4. A memory system according to Claim 1, wherein said one point from which said plurality of socket pins of said socket are branched is one point of said wiring on said mother board.

5. A memory system according to Claim 1, wherein said one point from which said plurality of socket pins of said socket are branched is connected to the wiring on said mother board by way of the wirings inside said socket.

6. A memory system according to Claim 1, wherein, of said plurality of socket pins of said socket, the pins for an address signal, a control signal, a data signal, and a data management signal are common to each of said plurality of memory modules, the pins for a clock signal, a clock management signal, a bank selecting signal, and a power supply signal are separated with each of said plurality of memory modules.

7. A memory system according to Claim 1, wherein termination resistors are not connected to said plurality of wirings on said mother board, or they are connected to one ends of said plurality of wirings, or they are connected to both ends of said plurality of wirings.

8. A memory system having a memory controller and plural memory modules connected by way of wirings on a mother board, the memory system satisfying the condition:

(difference of a distance between the nearest memory module and the farthest memory module, viewed from the memory controller) < (thickness of the memory module + thickness of

a mounted memory IC on said memory module) × (number of the memory modules - 1).

9. A memory system comprising:

a board,

a memory controller laid out on said board, and

a socket laid out on said board, on which plural memory modules can be mounted, wherein said memory controller is connected in an equal distance to each of said plural memory modules to be mounted on said socket.

10. A memory system comprising:

a board,

a memory controller laid out on said board, and

a connecting member laid out on said board, which includes a first mounting slot having a plurality of first terminals and a second mounting slot having a plurality of second terminals,

wherein a first memory module can be mounted on said first mounting slot so as to connect said plurality of first terminals of said first mounting slot to a plurality of a third terminals of said first memory module,

wherein a second memory module can be mounted on said second mounting slot so as to connect a plurality of said second terminals of said second mounting slot to a plurality of a fourth terminals of said second memory module, and

wherein a wiring distance between said memory controller and one terminal of said plurality of first terminals is substantially equal to a wiring distance between said memory controller and one terminal of said plurality of second terminals corresponding to said one terminal of said plurality of first terminals.

11. A memory system according to Claim 10, wherein both said one terminal of said plurality of first terminals and said one terminal of said plurality of second terminals corresponding to said one terminal of said plurality of first terminals are a data terminal.

12. A memory system comprising:

a board,

a control device laid out on said board, including a first terminal,

a connecting member laid out on said board, which includes a first mounting part having a second terminal and a second mounting part having a third terminal corresponding to said second terminal,

wherein a first memory module can be mounted on said first mounting part,

wherein a second memory module can be mounted on said second mounting part,

wherein said first memory module has a fourth terminal,

wherein said second memory module has a fifth terminal,

wherein, when said first memory module is mounted on said first mounting part, said second terminal is connected to said fourth terminal,

wherein, when said second memory module is mounted on said second mounting part, said third terminal is connected to said fifth terminal, and

wherein the shortest distance of wirings between said first terminal of said control device and said second terminal of said first mounting part is substantially equal to the shortest distance of wirings between said first terminal of said control device and said third terminal of said second mounting part.

13. A memory system according to Claim 12 or 13, wherein both said second terminal and said third terminal are a data terminal.

14. A memory system according to Claim 12 or 13,

wherein said connecting member comprises a sixth terminal,

wherein said board further comprises a first board wiring that connects said first terminal with said sixth terminal, and

wherein said connecting member further comprises a first

wiring member connected between said sixth terminal and said second terminal, and a second wiring member connected between said sixth terminal and said third terminal.

15. A memory system according to Claim 14, wherein a length of said first wiring member is substantially equal to a length of said second wiring member.

16. A memory system according to Claim 14,

wherein said connecting member is a socket,

wherein said first mounting part and said first wiring member constitute a first socket pin, and

wherein said second mounting part and said second wiring member constitute a second socket pin.

17. A memory system according to Claim 12, wherein, when said first memory module is mounted on said first mounting part and said second memory module is mounted on said second mounting part, said first memory module and said second memory module are laid out in a radial form.

18. A memory system according to Claim 12, wherein, when said first memory module is mounted on said first mounting part and said second memory module is mounted on said second mounting part, said first memory module and said second memory module

are laid out in parallel.

19. A memory system according to Claim 12,

wherein said first memory module further comprises a sixth terminal,

wherein said second memory module comprises a seventh terminal corresponding to said sixth terminal,

wherein said first mounting part further comprises an eighth terminal,

wherein said second mounting part further comprises a ninth terminal,

wherein, when said first memory module is mounted on said first mounting part, said sixth terminal is connected to said eighth terminal,

wherein, when said second memory module is mounted on said second mounting part, said seventh terminal is connected to said ninth terminal, and

wherein said control device further comprises a tenth terminal connected to said eighth terminal and an eleventh terminal connected to said ninth terminal.

20. A memory system according to Claim 19,

wherein said eighth terminal is a terminal to receive a first clock signal, and

wherein said ninth terminal is a terminal to receive a

second clock signal.

21. A memory system according to Claim 19,

wherein said eighth terminal is a terminal to receive a first chip selecting signal, and

wherein said ninth terminal is a terminal to receive a second chip selecting signal.

22. A memory system according to Claim 19,

wherein said eighth terminal is a terminal to receive a first clock enable signal, and

wherein said ninth terminal is a terminal to receive a second clock enable signal.

23. A memory system according to Claim 12, wherein a plurality of dynamic memory chips are mounted on said first memory module and said second memory module.

24. A memory system according to Claim 12, wherein said control device is a memory controller.

25. A connecting member comprising a first mounting part having a first terminal, a second mounting part having a second terminal corresponding to said first terminal, and a third terminal,

wherein a first memory module can be mounted on said first mounting part,

wherein a second memory module can be mounted on said second mounting part,

wherein said first memory module has a fourth terminal,

wherein said second memory module has a fifth terminal corresponding to said fourth terminal,

wherein, when said first memory module is mounted on said first mounting part, said first terminal is connected to said fourth terminal,

wherein, when said second memory module is mounted on said second mounting part, said second terminal is connected to said fifth terminal,

wherein said third terminal is connected to said first terminal of said first mounting part by a first wiring member,

wherein said third terminal is connected to said second terminal of said second mounting part by a second wiring member, and

wherein a length of said first wiring member is equal to a length of said second wiring member.

26. A connecting member according to Claim 25, wherein said connecting member is a memory module socket.

27. A connecting member according to Claims 25 and 26,

wherein said first mounting part and said first wiring member are a first socket pin, and

wherein said second mounting part and said second wiring member are a second socket pin.

28. A connecting member according to Claim 25, wherein said connecting member can be laid out on a mounting board.

29. A connecting member according to Claims 25 to 28, wherein both said first terminal and said second terminal are a data terminal.